MIPS® YAMON™ Errata

Document Number: MD00032
Revision 02.24
February 15, 2011

MIPS Technologies, Inc.
955 East Arques Avenue
Sunnyvale, CA 94085-4521

Copyright © 1999-2011 MIPS Technologies Inc. All rights reserved.

Copyright © 1999-2011 MIPS Technologies, Inc. All rights reserved.

Unpublished rights (if any) reserved under the copyright laws of the United States of America and other countries.

This document contains information that is proprietary to MIPS Technologies, Inc. ("MIPS Technologies"). Any copying, reproducing, modifying or use of this information (in whole or in part) that is not expressly permitted in writing by MIPS Technologies or an authorized third party is strictly prohibited. At a minimum, this information is protected under unfair competition and copyright laws. Violations thereof may result in criminal penalties and fines.

Any document provided in source format (i.e., in a modifiable form such as in FrameMaker or Microsoft Word format) is subject to use and distribution restrictions that are independent of and supplemental to any and all confidentiality restrictions. UNDER NO CIRCUMSTANCES MAY A DOCUMENT PROVIDED IN SOURCE FORMAT BE DISTRIBUTED TO A THIRD PARTY IN SOURCE FORMAT WITHOUT THE EXPRESS WRITTEN PERMISSION OF MIPS TECHNOLOGIES, INC.

MIPS Technologies reserves the right to change the information contained in this document to improve function, design or otherwise. MIPS Technologies does not assume any liability arising out of the application or use of this information, or of any error or omission in such information. Any warranties, whether express, statutory, implied or otherwise, including but not limited to the implied warranties of merchantability or fitness for a particular purpose, are excluded. Except as expressly provided in any written license agreement from MIPS Technologies or an authorized third party, the furnishing of this document does not give recipient any license to any intellectual property rights, including any patent rights, that cover the information in this document.

The information contained in this document shall not be exported, reexported, transferred, or released, directly or indirectly, in violation of the law of any country or international law, regulation, treaty, Executive Order, statute, amendments or supplements thereto. Should a conflict arise regarding the export, reexport, transfer, or release of the information contained in this document, the laws of the United States of America shall be the governing law.

The information contained in this document constitutes one or more of the following: commercial computer software, commercial computer software documentation or other commercial items. If the user of this information, or any related documentation of any kind, including related technical data or manuals, is an agency, department, or other entity of the United States government ("Government"), the use, duplication, reproduction, release, modification, disclosure, or transfer of this information, or any related documentation of any kind, is restricted in accordance with Federal Acquisition Regulation 12.212 for civilian agencies and Defense Federal Acquisition Regulation Supplement 227.7202 for military agencies. The use of this information by the Government is further restricted in accordance with the terms of the license agreement(s) and/or applicable contract terms and conditions covering this information from MIPS Technologies or an authorized third party.

MIPS, MIPS I, MIPS II, MIPS III, MIPS IV, MIPS V, MIPSr3, MIPS32, MIPS64, microMIPS32, microMIPS64, MIPS-3D, MIPS16, MIPS16e, MIPS-Based, MIPSsim, MIPSpro, MIPS Technologies logo, MIPS-VERIFIED, MIPS-VERIFIED logo, 4K, 4Kc, 4Km, 4Kp, 4KE, 4KEc, 4KEm, 4KEp, 4KS, 4KSc, 4KSd, M4K, M14K, 5K, 5Kc, 5Kf, 24K, 24Kc, 24Kf, 24KE, 24KEc, 24KEf, 34K, 34Kc, 34Kf, 74K, 74Kc, 74Kf, 1004K, 1004Kc, 1004Kf, 1074K, 1074Kc, 1074Kf, R3000, R4000, R5000, ASMACRO, Atlas, "At the core of the user experience.", BusBridge, Bus Navigator, CLAM, CorExtend, CoreFPGA, CoreLV, EC, FPGA View, FS2, FS2 FIRST SILICON SOLUTIONS logo, FS2 NAVIGATOR, HyperDebug, HyperJTAG, IASim, JALGO, Logic Navigator, Malta, MDMX, MED, MGB, microMIPS, OCI, PDtrace, the Pipeline, Pro Series, SEAD, SEAD-2, SmartMIPS, SOC-it, System Navigator, and YAMON are trademarks or registered trademarks of MIPS Technologies, Inc. in the United States and other countries.

All other trademarks referred to herein are the property of their respective owners.

Template: nB1.03, Built with tags: 2B

Copyright © 1999-2011 MIPS Technologies Inc. All rights reserved.

Copyright © 1999-2011 MIPS Technologies Inc. All rights reserved.

Preface

This document communicates errata for the YAMON™ ROM monitor.

This document also communicates errata for two special versions of YAMON:

- YAMON SEAD 01.00 ROM monitor.
- YAMON NOLAN 01.00 ROM monitor.

Both of these are identical to YAMON 01.00 except for the following:

- Ethernet LAN support has been removed.
- In the case of NOLAN, the E2 erratum has been fixed.

They are both obsoleted by YAMON 01.01 and later revisions.

The document consists of the following sections:

- Section 1, "Revisions" Provides information on YAMON revisions. A matrix shows the relation between the YAMON revisions and the Errata numbers.
- Section 2, "Errata" A detailed description of the YAMON errata, the implications, suggested workarounds, and status.
- Section 3, "Functional Changes" A description of functional changes made to YAMON. This section reflects new or modified functionality added to a particular version of YAMON, not errata.

The descriptions of the errata and the functional changes include information about the status of the errata/change. The codes listed in the following table are used to describe their status.

Table 1 Status Codes Used in the Descriptions of Errata and Changes

Code	Description
Open	This issue is under investigation.
Fixed	This issue has been fixed.
Fix	This issue is intended to be fixed in a future version of YAMON.
NoFix	There are no plans to fix this issue.
Added	This functionality has been added/modified.

Copyright © 1999-2011 MIPS Technologies Inc. All rights reserved.

1 Revisions

1.1 Revision Overview

Table 2 lists the revisions of YAMON.

Table 2 Summary of YAMON Revisions

YAMON Revision	Description	Date
01.00	Initial Release	Dec 14, 1999
01.01	New commands added (ping, scpu). Source code rearranged. Minor bug fixes.	Jan 31, 2000
02.00	Added support for Malta and SEAD-2 boards. New commands added (cache, sleep, tlb). Rearranged source code making YAMON easier to port to new platforms/ CPUs. Added "info isa" for Malta board. Support for high baud rates on Malta (230400bps, 460800bps). Optimized SDRAM configuration. Support for 64-bit user applications, including GDB stub. “gdb” command: Added verbose ("-v") and disable checksum ("-c") options as well as parameter passing to applications. Added retry ("-r") option to load command. Additions to the YAMON API: Registration of exception handlers. Getchar. SYSCON read (for access to various YAMON configuration data). Added “start” environment variable that is executed after a reset (unless cancelled). ";" separation of commands. If command line starts with +<n>; the line is repeated n times. Environment variables may now be used as "alias". Exception dump compressed, in particular on 64-bit processors. Improved check for address validity, including TLB lookup. Added EJTAG and NMI exception vectors.	Sep 11, 2000

Copyright © 1999-2011 MIPS Technologies Inc. All rights reserved.

Table 2 Summary of YAMON Revisions (Continued)

YAMON Revision	Description	Date
02.02	Support for 20Kc™, 4KEc™, 4KEm™, 4KEp™, 4KSc™, 5Kf™, QED RM7061A (including L2 cache support). Support for CoreFPGA™, CoreBonito64™, Core20K™ core cards. MIPS16e™, MIPS64™, MIPS3D™, FPU support in disassembly command ("dis"). MIPS16e™, FPU support in "gdb" command. Added "disk" command (IDE Harddisk/Compact Flash support). Added "cp1" command. Support for applications using FPU. Exception dump shows FPU registers. Cache command more general. Added '.' command for "dis", "dump" and "eeprom" commands. Added "dis" target for makefile (make dis). Code somewhat rearranged in order to make YAMON easier to port. Bugfixes (E4, E5, E6, E7).	July 27, 2001
02.03	Support for MIPS SOC-it 101 system controller on SEAD-2. Support for 256 MByte SDRAM on CoreLV™ and CoreFPGA™ core cards. Added FPU emulator. Added "fpu", "fread", "fwrite" and "info sysctrl" commands. YAMON boots even though PCI resource allocation fails. YAMON revision shown in display as [YAMON203]. Bugfixes (E8, E9, E10).	Aug 14, 2002
02.04	dis command now supports MIPS32/MIPS64 Release 2 instructions. tlb command now supports 1kB pages for MIPS32/MIPS64 Release 2 CPUs supporting small pages. In general CP0 registers are now accessed using 32 or 64-bit operations depending on actual width of register. cp0 command and exception handling updated so that only CP0 registers available for the particular CPU are accessed. Added support for MIPS32/MIPS64 Release 2 CPU shadow register sets. Added support for MIPS M4K, 4KSd, 5KE, 5KEf, 25Kf CPUs. Added support for CoreFPGA-2 Core card. Bugfix (E12).	Nov 21, 2002
2.05	Added support for CoreFPGA rev2 Core card. Added support for MIPS 24K CPUs. BugFix (E13, E14)	Dec 13, 2003
2.06	BugFix (E15, E16)	Mar 23, 2004
2.07	Added EIC support Improved environment variable handling Added support for GCC 3.x BugFix (E17)	
2.08	Added support for MT and DSP ASE BugFix (E18)	31 Feb, 2005
2.09	BugFix (E19)	15 Jun, 2005
2.10	Added CoreFPGA-3 support	14 Oct, 2005

Copyright © 1999-2011 MIPS Technologies Inc. All rights reserved.

Table 2 Summary of YAMON Revisions (Continued)

YAMON Revision	Description	Date
2.11	BugFix (E20)	16 Feb, 2006
2.12	Added support for Core24KLV, 74K and MIPS L2 cache BugFix (E21, E22, E23)	4 Jul, 2006
2.13	Additional SOCit support, 24KE cache support (F58, F59) BugFixes (E24, E25, E26)	
2.14	Added support for new Interrupt controller (GIC) and software endianness selection on RoHS compliant revisions of the Malta board (F60, F61).	11 Nov, 2007
2.15	Added support for CMP operation (F62)	30 Nov, 2007
2.16	Updated CMP support (F62). BugFix (E27, E28) Issues (E29)	23 Jun, 2008
2.17	BugFixes (E30, E31, E32, E33, E34, E35, E36, E37, E38) Added 74KLV board support (F63), added CPC support (F64), added microMIPS support (F65), added SEAD-3 board support (F66, F70, F71, F72, F73, F74), use highest CAS latency during boot (F67), added display of additional clock rate multipliers (F68), added new support routine for gcc4 (F69), added L2 cache resizing support (F75), added message for DSP/MDMX unusable exception (F76).	6 Nov, 2009
2.18	Updated SEAD-3 support (F77-F84). BugFix (E39)	2 October, 2010
2.19	Added support for 4K caches and 1074K CPU (F85-86). BugFix (E40)	3 August, 2010
2.20	Add1 Gigabyte and 2 Gigabyte DIMM support (F87), change PAUSE_COUNT to permit I2C interface to work with 1GHz processors (F88), add DDR/ECC build when RMW function is turned off for CPU write bursts (F89), enhance RTC initialization (F90), modify PIC32 to function with a 250MHz core on SEAD-3 boards (F91).	15 February, 2011

Table 3 lists the revisions of YAMON SEAD.

Table 3 Summary of YAMON SEAD Revisions

YAMON SEAD Revision	Description	Date
01.00	Initial Release. Identical to YAMON 01.00 except for the following: Ethernet LAN support has been removed.	Jan 7, 1999

Table 4 lists the revisions of YAMON NOLAN.

Copyright © 1999-2011 MIPS Technologies Inc. All rights reserved.

Table 4 Summary of YAMON NOLAN Revisions

YAMON NOLAN Revision	Description	Date
01.00	Initial Release. Identical to YAMON 01.00 except for the following: Ethernet LAN support has been removed. Erratum E2 has been fixed.	Jan 13, 1999

Copyright © 1999-2011 MIPS Technologies Inc. All rights reserved.

1.2 Overview of Errata and Functional Changes

Table 5 and Table 6 provide a one-line overview of the YAMON Errata and the Functional Changes. Each of these are assigned a unique name/number.

Table 5 Summary of YAMON Errata

YAMON Erratum No	Description
E1	YAMON does not compile using Algorithmics SDE tools.
E2	copy command does not flush caches before copying.
E3	DMA not disabled before starting user application.
E4	GDB “load” command fails.
E5	GDB register transfer in little endian.
E6	No 64-bit sign extension of a2 passed to user application.
E7	Calling YAMON API with KSU field of STATUS register = 01 (Supervisor mode) fails.
E8	YAMON 02.02 may fail on 5Kf due to FPU hazard.
E9	YAMON 02.02 may fail on 20K due to missing data cache tag initialization.
E10	YAMON 02.02 TFTP client does not work against RedHat Linux 7.3 TFTP server.
E11	YAMON 02.03 FPU emulator wrong for mfc1 instruction on 64-bit CPUs.
E12	GDB breakpoint causes loss of all the application’s registered exception handlers.
E13	YAMON 02.04 with SOC-it fails memory accesses from PCI above 16Mbyte.
E14	YAMON does not restore $gp register when calling registered interrupt handler.
E15	YAMON does not write back entire L2 cache.
E16	YAMON 2.05 fails to initialize on SEAD.
E17	Buffer overrun in eeprom help command
E18	Buffer overrun in info IDE command
E19	Enhanced NMI handling
E20	24K/34K data cache initial is at ion
E21	EXCEP_return not restoring k1
E22	Initialisation of parity memory
E23	Software configuration of cache sizes
E24	Corrections to Galileo memory configuration
E25	Avoid downloading into memory used by YAMON
E26	Allow the MIPS L2 cache to be bypassed correctly
E27	Corrected cp0 command

Copyright © 1999-2011 MIPS Technologies Inc. All rights reserved.

Table 5 Summary of YAMON Errata (Continued)

YAMON Erratum No	Description
E28	Cache command
E29	ROCit system controller setup
E30	Timing calculations
E31	Bus ratio setting
E32	Parity initialization
E33	Big endian return status
E34	Unaligned default stack address
E35	EHB to NOP
E36	Ack on last tftp block
E37	ARP time-out
E38	Byte alignment for microMIPS toolchains
E39	scpu -p option
E40	D-cache flush on memory allocation

Table 6 Summary of Functional Changes

Functional Change No	Description
F1	“ping” command added.
F2	“scpu” command added.
F3	Source code restructured.
F4	Added support for Malta and SEAD-2 boards.
F5	“cache” command added.
F6	“sleep” command added.
F7	“tlb” command added.
F8	Added “info isa” (Malta only).
F9	Support for 230400bps and 460800bps on tty0/tty1 (Malta only).
F10	Optimized SDRAM configuration (Atlas and Malta).
F11	Support for 64-bit user applications (including GDB support).
F12	“gdb” command: Added “-v”, “-c” options and added support for passing parameters to application being debugged.
F13	Added “-r” option to load command.

Copyright © 1999-2011 MIPS Technologies Inc. All rights reserved.

Table 6 Summary of Functional Changes (Continued)

Functional Change No	Description
F14	Additions to YAMON API: Registration of exception handlers Getchar SYSCON read
F15	Added “start” environment variable that is executed after a reset (unless cancelled).
F16	";" separation of commands.
F17	If command line starts with +<n>; the line is repeated n times.
F18	Environment variables may now be used as "alias".
F19	Exception dump compressed, in particular on 64-bit processors.
F20	Improved check for address validity, including TLB lookup.
F21	Added EJTAG and NMI exception vectors.
F22	Support for 20Kc™, 4KEc™, 4KEm™, 4KEp™, 4KSc™, 5Kf™, QED RM7061A (including L2 cache support).
F23	Support for CoreFPGA™, CoreBonito64™, Core20K™ core boards.
F24	MIPS16e™, MIPS64™, MIPS3D™, FPU support in disassembly command ("dis").
F25	MIPS16e™, FPU support in "gdb" command.
F26	Added "disk" command (IDE Harddisk/Compact Flash support).
F27	Added "cp1" command.
F28	Support for applications using FPU.
F29	Exception dump shows FPU registers.
F30	Cache command modified.
F31	Added ’.’ command for "dis", "dump" and "eeprom" commands.
F32	Added "dis" target for makefile (make dis).
F33	Code somewhat rearranged in order to make YAMON easier to port.
F34	Support for CoreSYS™ core boards and SOC-it 101™ system controller on SEAD-2.
F35	Added FPU emulator, fpu command and "fpu" environment variable to control emulator after reset.
F36	Added "fread" and "fwrite" commands
F37	Added "info sysctrl" command.
F38	YAMON is restarted after register dump.
F39	Added “startdelay” environment variable to control invocation of "start" command.
F40	dis command now supports MIPS32/MIPS64 Release 2 instructions.

Copyright © 1999-2011 MIPS Technologies Inc. All rights reserved.

Table 6 Summary of Functional Changes (Continued)

Functional Change No	Description
F41	tlb command now supports 1kB pages for MIPS32/MIPS64 Release 2 CPUs supporting small pages.
F42	In general CP0 registers are now accessed using 32 or 64-bit operations depending on actual width of register.
F43	cp0 command and exception handling updated so that only CP0 registers available for the particular CPU are accessed.
F44	Added support for MIPS32/MIPS64 Release 2 CPU shadow register sets.
F45	Added support for MIPS M4K, 4KSd, 5KE, 5KEf, 25Kf CPUs.
F46	Added support for CoreFPGA-2 Core card.
F47	Added support for CoreFPGA rev2 Core Card
F48	Added support for MIPS 24K
F49	Added support for external interrupt controller (EIC)
F50	Improved parsing of environment variables
F51	Support GCC for version 3.x
F52	Added MT/DSP ASE support
F53	Added MIPS 24KE support
F54	Added CoreFPGA-3 support
F55	Added Core24KLV support
F56	Added MIPS 74K support
F57	Added MIPS L2 cache support
F58	Additional SOCit support
F59	Added 24KE cache support
F60	Added GIC support for RoHS Malta boards
F61	Added support for software endian selection on RoHS Malta boards
F62	Added CMP support
F63	Added 74KLV board support
F64	Added CPC support
F65	Added microMIPS support
F66	Added SEAD-3 board support
F67	Use highest CAS latency during boot.
F68	Added display of additional clock rate multipliers
F69	Added new support routine for gcc4

Copyright © 1999-2011 MIPS Technologies Inc. All rights reserved.

Table 6 Summary of Functional Changes (Continued)

Functional Change No	Description
F70	Added NEWSC switch interrupt handling for SEAD-3 boards
F71	Added SOFTENDIAN support for SEAD-3 boards
F72	Added SOFTEIC support for SEAD-3 boards
F73	Added RTC support for SEAD-3 boards
F74	Added GIC support for SEAD-3 boards
F75	Added L2 cache resizing support
F76	Added message for DSP/MDMX unusable exception
F77	Added ASET and ACLR testing for SEAD-3 boards
F78	Added I_SRAM and D_SRAM support to SEAD-3 boards
F79	Added secondary boot loader for SEAD-3 boards
F80	Added code to allow resetting of PIC32 chip via reset register on SEAD-3 boards
F81	Changed the default TTY port (ttyS0) to be the USB serial port for SEAD-3 boards
F82	Added code to allow user to select the TTY port via the NEWSC buttons on SEAD-3 boards
F83	Added code for resetting all environment variables to default via NEWSC buttons on SEAD-3 boards
F84	Added hardware monitoring via ADT7476 chip on SEAD-3 boards
F85	Added support for 4K cache and 1074K
F86	Added 2 perl scripts used in the release process
F87	Added 1 Gigabyte and 2 Gigabyte DIMM support.
F88	Changed PAUSE_COUNT to permit I2C interface to work with 1GHz processors
F89	Added DDR/ECC build when RMW function is turned off for CPU write bursts
F90	Enhanced RTC initialization
F91	Modified PIC32 to function with a 250MHz core on SEAD-3 boards

1.3 YAMON Revisions and Errata/Changes

The tables below correlate each erratum or functional change to specific revisions of YAMON / YAMON NOLAN. The errata or changes are divided into two groups:

- YAMON Errata. This group shows errata for YAMON. Each YAMON erratum has a tracking number identified with the prefix “E”. An “X” in the square for a particular revision column indicates that specific revision contains the erratum. If the square is blank, then the erratum is not present in that specific revision.
- Functional Changes. The final group shows the functional changes which have been made to YAMON. Functional changes are identified with the prefix “F”. Here, an “X” in the square for a particular revision column indicates that

Copyright © 1999-2011 MIPS Technologies Inc. All rights reserved.

specific revision contains the functional change. If the square is blank, then the functional change is not present in that specific revision.

Table 7 Relation between YAMON Revisions and Errata Number

	YAMON Revision										
	1.00	**1.01**	**2.00**	**2.02**	**2.03**	**2.04**	**2.05**	**2.06**	**2.07**	**2.08**	**2.09**
Errata											
E1	X										
E2	X										
E3	X										
E4			X								
E5			X								
E6	X	X	X								
E7	X	X	X								
E8				X							
E9				X							
E10				X							
E11					X						
E12	X	X	X	X	X						
E13						X					
E14			X	X	X	X					
E15							X				
E16							X				
E17			X	X	X	X	X	X			
E18			X	X	X	X	X	X	X		
E19			X	X	X	X	X	X	X	X	
E20							X	X	X	X	X
E21		X	X	X	X	X	X	X	X	X	X
E22					X	X	X	X	X	X	X
E23		X	X	X	X	X	X	X	X	X	X
E24											
E25											
E26											
E27											

Copyright © 1999-2011 MIPS Technologies Inc. All rights reserved.

Table 7 Relation between YAMON Revisions and Errata Number (Continued)

	YAMON Revision										
	1.00	**1.01**	**2.00**	**2.02**	**2.03**	**2.04**	**2.05**	**2.06**	**2.07**	**2.08**	**2.09**
E28											
E29											
Changes											
F1		X	X	X	X	X					
F2		X	X	X	X	X					
F3		X	X	X	X	X					
F4			X	X	X	X					
F5			X	X	X	X					
F6			X	X	X	X					
F7			X	X	X	X					
F8			X	X	X	X					
F9			X	X	X	X					
F10			X	X	X	X					
F11			X	X	X	X					
F12			X	X	X	X					
F13			X	X	X	X					
F14			X	X	X	X					
F15			X	X	X	X					
F16			X	X	X	X					
F17			X	X	X	X					
F18			X	X	X	X					
F19			X	X	X	X					
F20			X	X	X	X					
F21			X	X	X	X					
F22				X	X	X					
F23				X	X	X					
F24				X	X	X					
F25				X	X	X					
F26				X	X	X					
F27				X	X	X					

Copyright © 1999-2011 MIPS Technologies Inc. All rights reserved.

Table 7 Relation between YAMON Revisions and Errata Number (Continued)

	YAMON Revision										
	1.00	**1.01**	**2.00**	**2.02**	**2.03**	**2.04**	**2.05**	**2.06**	**2.07**	**2.08**	**2.09**
F28				X	X	X					
F29				X	X	X					
F30				X	X	X					
F31				X	X	X					
F32				X	X	X					
F33				X	X	X					
F34					X	X					
F35					X	X					
F36					X	X					
F37					X	X					
F38					X	X					
F39					X	X					
F40						X					
F41						X					
F42						X					
F43						X					
F44						X					
F45						X					
F46						X					
F47							X				
F48							X				
F49									X		
F50									X		
F51									X		
F52										X	

Copyright © 1999-2011 MIPS Technologies Inc. All rights reserved.

	YAMON Revision										
	2.10	**2.11**	**2.12**	**2.13**	**2.14**	**2.15**	**2.16**	**2.17**	**2.18**	**2.19**	**2.20**
Errata											
E18											
E19											
E20	X										
E21	X	X	X								
E22	X	X	X								
E23	X	X	X								
E24				X	X						
E25				X	X						
E26				X	X						
E27				X	X	X					
E28				X	X	X					
E29				X	X	X	X				
E30								X			
E31								X			
E32								X			
E33								X			
E34								X			
E35								X			
E36								X			
E37								X			
E38								X			
E39									X		
E40										X	
Changes											
F50											
F51											
F52											
F53	X										
F54	X										

Copyright © 1999-2011 MIPS Technologies Inc. All rights reserved.

	YAMON Revision										
	2.10	**2.11**	**2.12**	**2.13**	**2.14**	**2.15**	**2.16**	**2.17**	**2.18**	**2.19**	**2.20**
F55			X								
F56			X								
F57			X								
F58				X							
F59				X							
F60					X						
F61					X						
F62						X					
F63								X			
F64								X			
F65								X			
F66								X			
F67								X			
F68								X			
F69								X			
F70								X			
F71								X			
F72								X			
F73								X			
F74								X			
F75								X			
F76								X			
F77									X		
F78									X		
F79									X		
F80									X		
F81									X		
F82									X		
F83									X		
F84									X		
F85										X	

Copyright © 1999-2011 MIPS Technologies Inc. All rights reserved.

	YAMON Revision										
	2.10	2.11	2.12	2.13	2.14	2.15	2.16	2.17	2.18	2.19	2.20
F86										X	
F87											X
F88											X
F89											X
F90											X
F91											X

Table 8 Relation between YAMON SEAD Revisions and Errata Number

	YAMON SEAD Revision								
	01.00								
YAMON Errata									
E1	X								
E2	X								
E3	X								
E4									
E5									
E6	X								
E7	X								
Functional Changes									

Table 9 Relation between YAMON NOLAN Revisions and Errata Number

	YAMON NOLAN Revision								
	01.00								
YAMON Errata									
E1	X								
E2									
E3	X								
E4									

Copyright © 1999-2011 MIPS Technologies Inc. All rights reserved.

Table 9 Relation between YAMON NOLAN Revisions and Errata Number (Continued)

	YAMON NOLAN Revision								
	01.00								
E5									
E6	X								
E7									
Functional Changes									

Copyright © 1999-2011 MIPS Technologies Inc. All rights reserved.

2 Errata

E1 YAMON does not compile using Algorithmics SDE tools.

Problem: SDE tools do not accept ".bss" in assembler files, but require ".section bss".

Implication: Fix errors before using SDE tools.

Workaround: Replace ".bss" with ".section bss". However, then it will not work using Cygnus GCC.

Status: Fixed (in revision 01.01).

E2 Copy command does not flush cashes before copying.

Problem: YAMON flushes caches after the copy operation, but not before.

Implication: When copying data to uncached memory (KSEG1), data may be overwritten by hardware if caches lines are dirty and later evicted.

Workaround: User should perform the shell command "flush -d" before copying to uncached address (KSEG1).

Status: Fixed (in revision 01.01).

E3 DMA not disabled before starting user application.

Problem: YAMON "go" command does not disable DMA before starting user application.

Implication: If user application attempts to take-over the entire RAM space including the low range used by YAMON, data may be overwritten due to DMA from the Ethernet controller (only on boards supporting Ethernet).

Workaround: User application should not take-over YAMON RAM unless it first disables DMA from Ethernet controller (only on boards supporting Ethernet).

Status: Fixed (in revision 01.01).

E4 GDB "load" command fails.

Problem: YAMON rejects "move to memory" (M) command from GDB if byte count > 255. This will occur when the GDB "load" command is used for files that are larger than 255 bytes.

Implication: GDB "load" will not function.

Workaround: Use YAMON to load application. Then connect to GDB and jump to application start address (using the GDB "jump" command).

Status: Fixed (in revision 02.02).

Copyright © 1999-2011 MIPS Technologies Inc. All rights reserved.

E5 GDB register transfer in little endian.

Problem: YAMON misinterprets register value in the “write single register” (P) command when running in little endian mode. This will occur when the GDB “load” command is used.

Implication: GDB “load” will not function in little endian mode.

Workaround: Use YAMON to load application. Then connect to GDB and jump to application start address (using the GDB “jump” command).

Status: Fixed (in revision 02.02).

E6 No 64-bit sign extension of a2 passed to user application.

Problem: When an application is started using "go" or "gdb" commands, a2 points to an array holding the YAMON environment variables. When executing on a 64-bit CPU, the 32 msb of a2 must be sign-extended. This does not happen.

Implication: User applications executing on a 64-bit CPU may not use contents of a2 passed by YAMON unmodified.

Workaround: User application must sign extend a2 before using it. It could for example do the following:

```
addiu a2, 0
```

Status: Fixed (in revision 02.02).

E7 Calling YAMON API with KSU field of STATUS register = 01 (Supervisor mode) fails.

Problem: When an application uses the YAMON API to for example print a string to the display, YAMON will clear bit 4 of CP0 STATUS register before clearing EXL and ERL. However, if bit 3 indicates Supervisor mode rather than Kernel mode, clearing EXL, ERL will cause CPU to enter Supervisor mode, so next KSEG0 access or mfc0 instruction will cause an exception.

Implication: An exception will be taken when using the YAMON API.

Workaround: Set KSU to 00 (Kernel mode) before calling YAMON API functions.

Status: Fixed (in revision 02.02).

E8 YAMON 02.02 may fail on 5Kf due to FPU hazard.

Problem: The 5Kf CPU requires 4 instructions between setting CU1 bit (thus enabling FPU) and performing the first FPU instruction. YAMON 02.02 only has 3 "nop" instructions, which may cause YAMON to take an exception and stall. This bug only occurs in YAMON 02.02.

Implication: An exception may be taken during YAMON initialization causing YAMON to stall.

Workaround: None.

Status: Fixed (in revision 02.03).

Copyright © 1999-2011 MIPS Technologies Inc. All rights reserved.

E9 YAMON 02.02 may fail on 20Kc due to missing data cache tag initialization.

Problem: The 20Kc CPU requires its separate data cache tags to be initialized. This bug only occurs in YAMON 02.02.

Implication: Dependent on 20Kc implementation: most likely none with 20Kc in silicon, but will prevent YAMON from starting in simulation environment.

Workaround: None.

Status: Fixed (in revision 02.03).

E10 YAMON 02.02 TFTP client does not work against RedHat Linux 7.3 TFTP server.

Problem: The TFTP client of YAMON up to and including revision 02.02 implements a flow control scheme, where TFTP-ACK means that the current data packet has been received, but there may not be room for next data packet which is then discarded by the client. When later room for the next data packet becomes available, the client resends TFTP-ACK in order for the TFTP server to resend the last data packet. RedHat Linux-7.3 tftp-hpa server does not retransmit because of a second reception of an TFTP-ACK, and eventually YAMON times out and closes down the session.

Implication: TFTP loads time out.

Workaround: None.

Status: Fixed (in revision 02.03) by a new flow control scheme, where TFTP-ACK means that A) the current data packet has been received and B) there is room for another data packet.

E11 E11. YAMON 02.03 FPU emulator wrong for mfc1 instruction on 64-bit CPUs.

Problem: When the built-in FPU emulator is used to emulate an mfc1 instruction, the upper 32-bits are left undefined. This is only relevant for processors with 64-bit registers.

Implication: Subsequent comparison against integer registers may not work as expected.

Workaround: None.

Status: Fixed (in revision 02.04).

E12 GDB breakpoint causes loss of all the application's registered exception handlers.

Problem: When an application has registered any exception of any type, the corresponding pointer inside YAMON is overwritten as soon as a GDB breakpoint is reached.

Implication: Subsequent exceptions are not redirected to the application, rather swallowed by YAMON. That makes it impossible to use GDB to debug applications after the first exception registration and until the last deregistration.

Workaround: None.

Status: Fixed (in revision 02.04).

Copyright © 1999-2011 MIPS Technologies Inc. All rights reserved.

E13 YAMON 02.04 with SOC-it fails memory accesses from PCI above 16Mbyte.

Problem: Main memory accesses from the PCI side above 16Mbyte hit the low 16Mbyte due to incorrect configuration of the SOC-it 101 system controller.

Implication: This error is never seen with YAMON itself, as YAMON uses less than 1 Mbyte of memory, but will cause unpredictable behavior if an operating system use some pci device with DMA to/from a location above 16Mbyte.

Workaround: After YAMON is booted (for instance as part of the "start" environment), this YAMON command fixes the error:

```
YAMON> port bbd00308 f0000000
```

Status: Fixed (in all revisions after 02.04).

E14 YAMON does not restore $gp register when calling registered interrupt handler.

Problem: An application that uses $gp for GP relative addressing can register an interrupt handler with YAMON, but YAMON will call the interrupt handler with $gp set to the YAMON data area.

Implication: Application interrupt handlers will not be able to access data/variables using GP relative addressing.

Workaround: Do not use GP relative addressing in interrupt handlers that will be called from YAMON.

Status: Fixed (in revision 02.05).

E15 YAMON does not write back entire L2 cache.

Problem: The YAMON flush command does a writeback and invalidate on a selected address range in the L2 cache. This can leave data in the L2 cache that has not been written back to memory.

Implication: In most cases this does not affect correct operation of YAMON. The L2 cache will be written back to memory as required. This behavior can lead to unexpected results if memory is written through the L2 cache, flushed and then examined using uncached addresses.

A more serious problem occurs if an application is loaded into memory which when executed reinitializes the L2 cache without writing it back to memory. This can lead to the use of stale data by the application.

Workaround: After downloading application, write sufficient data to an unused section of memory to cause the entire L2 cache to be written back to memory:

```
YAMON> fill -32 0x9fc00000 0x10000 0
```

Status: Fixed (in revision 02.06).

E16 YAMON 2.05 fails to initialize on SEAD.

Problem: YAMON 2.05 does not initialize correctly on SEAD.

Workaround: Do not use YAMON 2.05 on SEAD.

Copyright © 1999-2011 MIPS Technologies Inc. All rights reserved.

Status: Fixed (in revision 02.06).

E17 Buffer overrun in eeprom help command

Problem: The help string for the eeprom command was corrupted due to a buffer overrun.

Status: Fixed (in revision 02.07).

E18 Buffer overrun in info ide command

Problem: The "info ide" command was corrupting the stack when more that one device was present on the IDE bus.

Status: Fixed (in revision 02.08)

E19 Enhanced NMI handling

Problem: The reset handler modified some processor state while handling an NMI.

Implication: The register contents reported by the NMI handler did not accurately reflect the processor state when the NMI occurred

Status: Fixed (in revision 02.09)

E20 24K/34K data cache initialization

Problem: YAMON did not clear the DTagLo register when initializing the data cache.

Implication: The value written to the data cache tags during initialization was essentially random. This could cause problems if the tag was written as valid.

Status: Fixed (in revision 02.11)

E21 EXCEP_return not restoring k1

Problem: An application calling EXCEP_return could crash

Implication: If an application called EXCEP_return because it did not want to handle an exception, YAMON would not reload $k1 which would prevent it from handling further exceptions correctly.

Workaround: For backwards compatibility, applications should preserve the $k1 register while running registered exception handlers if they may later call EXCEP_return.

Status: Fixed (in revision 2.12)

E22 Initialization of parity memory

Problem: Using parity memory could cause an NMI

Copyright © 1999-2011 MIPS Technologies Inc. All rights reserved.

Implication: Parity checking was not being disabled while initializing parity protected memory. If the system controller performed a read-modify-write during memory initialization an NMI could occur.

Status: Fixed (in revision 02.12)

E23 Software configuration of cache sizes

Problem: The available cache configurations reported by the *scpu* command were incorrect when the I & D cache sizes differed.

Implication: Not all possible cache configurations could be used.

Status: Fixed (in revision 02.12)

E24 Corrections to Galileo memory configuration

Problem: The Galileo memory controller was not being configured correctly

Implication: The memory controller was remaining in its default state which may not be correct for an arbitrary SDRAM module

Status: Fixed (in revision 02.13)

E25 Avoid downloading into memory used by YAMON

Problem: The address range checking performed on downloads was incomplete and allowed YAMON to overwrite code and data used by YAMON.

I**mplication**: It was possible to crash YAMON by downloading to an address that was being used by YAMON

Status: Fixed (in revision 02.13)

E26 Allow the MIPS L2 cache to be bypassed correctly

Problem: The cache command was not disabling the MIPS L2 cache

Implication: It was not possible to disable the L2 cache using the YAMON command line

Status: Fixed (in revision 02.13)

E27 Corrected cp0 command

Problem: YAMON was using some register names that were inconsistent with the MIPS32 architecture documentation. In addition the reading CP0 registers could occasionally return incorrect values due to incorrect handling of hazards.

Implication: Unconventional register names were being used. Any automated scripts that rely on these names will have to be updated.

Status: Fixed (in revision 02.16)

Copyright © 1999-2011 MIPS Technologies Inc. All rights reserved.

E28 Cache command

Problem: YAMON supports cache resizing for debug and testing purposes. On some cores it was allowing unsupported cache sizes to be selected.

Implication: Selecting cache sizes that are not supported by the core could lead to unreliable behavior.

Status: Fixed (in revision 02.16)

E29 ROCit system controller setup

Problem: With some exceptions (notably refresh timing) YAMON configures the memory system as if it is running at PC133 bus speeds regardless of the actual bus speed. The rationale for this is to mimic the behavior of a system running at full bus speed.

Implication: When benchmarking memory bound programs on Malta the behavior of the memory subsystem must be taken into account when interpreting results. The default setup can lead to lower than expected results.

Status: Open

E30 Timing calculations

Problem: Timing calculations incorrectly rounding TRP/TRAS/TRCD values.

Status: Fixed (in revision 02.17)

E31 Bus ratio setting

Problem: 74KLV does not correctly report 6:1 bus ratio setting. Use a switch on the board to fix up the reported value and settings.

Status: Fixed (in revision 02.17)

E32 Parity initialization

Problem: Parity initialization missing last word in memory.

Status: Fixed (in revision 02.17)

E33 Big Endian return status

Problem: 32-bit return status for Big Endian problem.

Status: Fixed (in revision 02.17)

E34 Unaligned default stack address

Problem: Default stack address unaligned on processors with hardware anti-alias support.

Copyright © 1999-2011 MIPS Technologies Inc. All rights reserved.

Status: Fixed (in revision 02.17)

E35 NOP

Problem: Convert nop into EHB.

Status: Fixed (in revision 02.17)

E36 Ack on last tftp block

Problem: No ack to the last tftp block.

Status: Fixed (in revision 02.17)

E37 ARP timeout

Problem: ARP timeout problems.

Status: Fixed (in revision 02.17)

E38 Byte alignment for microMIPS toolchains

Problem: Byte alignment bug for microMIPS toolchains.

Status: Fixed (in revision 02.17)

E39 scpu -p option doesn’t work if L2 cache is not present

Problem: This problem occurs only in YAMON versions with the L2 resizing feature.

Status: Fixed (in revision 02.18)

E40 D-cache not flushed when allocating memory

Problem: Coherency not maintained when memory is allocated and the D-cache has not been flushed.

Status: Fixed (in revision 02.19)

Copyright © 1999-2011 MIPS Technologies Inc. All rights reserved.

3 Functional Changes

F1 "ping" command added

Description: Added ping command on boards supporting Ethernet.

Status: Added (to revision 01.01).

F2 "scpu" command added

Description: Added scpu command for configurable CPUs.

Status: Added (to revision 01.01).

F3 Source code restructured

Description: Restructured source code and makefile structure.

Status: Added (to revision 01.01 and again in revision 02.00).

F4 Added support for Malta and SEAD-2 boards.

Description: YAMON now supports Malta and SEAD-2 boards.

Status: Added (to revision 02.00).

F5 "cache" command added.

Description: Added cache command for enabling/disabling cache (by setting K0 field of CP0 CONFIG register).

Status: Added (to revision 02.00).

F6 "sleep" command added.

Description: Added sleep command for halting YAMON the specified number of ms.

Status: Added (to revision 02.00).

F7 "tlb" command added.

Description: vd (to revision 02.00).

F8 Added "info isa" (Malta only).

yardsticks: Added "isa" as target for "info" command. This is used for displaying the memory mapping of devices on the ISA bus (Malta only).

Copyright © 1999-2011 MIPS Technologies Inc. All rights reserved.

Status: Added (to revision 02.00).

F9 Support for 230400bps and 460800bps on tty0/tty1 (Malta only).

Description: Malta supports 230400bps and 460800bps on tty0 and tty1.

Status: Added (to revision 02.00).

F10 Optimized SDRAM configuration (Atlas and Malta).

Description: North Bridge SDRAM configuration is optimized based on bus frequency.

Status: Added (to revision 02.00).

F11 Support for 64-bit user applications (including GDB support).

Description: Context shift now supports 64bit registers. Also, GDB extensions for 64-bit commands used by SDE-GDB from Algorithmics are now supported.

Status: Added (to revision 02.00).

F12 "gdb" command: Added "-v", "-c" options and added support for passing parameters to application being debugged.

Description: Added "-v" (verbose) option to "gdb" command. "-v" will cause commands from the GDB host and responses from YAMON to be displayed on tty0.

Added "-c" (Checksum disable) option to "gdb" command. "-c" will cause checksums in commands from the GDB host to be ignored.

Added support for passing parameters to application being debugged.

Status: Added (to revision 02.00).

F13 Added "-r" option to load command.

Description: Added "-r" (retry) option to load command.

This will cause load to retry on ARP timeouts.

Status: Added (to revision 02.00).

F14 Additions to YAMON API (Registration of exception handlers, Getchar, SYSCON read).

Description: Added support for registering Exception Service Routines (ESR), called when specific exceptions occur. Also added support for registering Interrupt Service Routines (ISR), called when an interrupt exception occurs due to either a CPU interrupt or an interrupt from the interrupt controller.

Added "getchar" function for receiving a character from tty0.

Copyright © 1999-2011 MIPS Technologies Inc. All rights reserved.

Added “syscon” function for reading internal YAMON configuration objects.

Status: Added (to revision 02.00).

F15 Added “start” environment variable that is executed after a reset (unless cancelled).

Description: An environment variable “start” now exists (default empty string). If not an empty string, the variable is executed following a reset unless cancelled by user (by pressing Ctrl-C within 2 seconds after YAMON requests him to).

Status: Added (to revision 02.00).

F16 ";" separation of commands.

Description: A command line may now contain several subcommands separated by “;”.

Example:

```
YAMON> echo abc; echo def
abc
def
YAMON>
```

Status: Added (to revision 02.00).

F17 If command line starts with +<n>; the line is repeated n times.

Description: A command line may now be repeated <n> times by adding +<n> as first subcommand.

Example:

```
YAMON> +2; echo abc
abc
abc
YAMON>
```

Status: Added (to revision 02.00).

F18 Environment variables may now be used as "alias".

Description: An environment variable may now be used as “alias” since it is now expanded before performing “;” separation

Example:

```
YAMON> setenv x “echo abc; echo def”
YAMON> $x
abc
def
YAMON>
```

Status: Added (to revision 02.00).

Copyright © 1999-2011 MIPS Technologies Inc. All rights reserved.

F19 Exception dump compressed, in particular on 64-bit processors.

Description: Exception dump is compressed to avoid data scrolling off the terminal (24 line terminal assumed).

Status: Added (to revision 02.00).

F20 Improved check for address validity, incl. TLB lookup.

Description: Addresses are now validated before an operation is performed. This includes alignment and, in case of a mapped address, TLB setup.

In case of RAM address space, it is verified that RAM is available for the access. For example, if the platform supports 128 MB RAM, and a 64 MB RAM module is used, only the first 64 MB are available.

Status: Added (to revision 02.00).

F21 Added EJTAG and NMI exception vectors.

Description: If hardware detects an EJTAG or NMI exception, it will jump to vector locations in flash/(E)PROM (0xbfc00480 and 0xbfc00000). YAMON has installed code at these vectors that jumps to RAM addresses 0x80000300 / 0x80000380. Code is further installed at these RAM vector locations jumping to the YAMON exception handling function, but a user application may overwrite the vector locations and take control of EJTAG and NMI exceptions.

Status: Added (to revision 02.00).

F22 Support for 20Kc™, 4KEc™, 4KEm™, 4KEp™, 4KSc™, 5Kf™, QED RM7061A (including L2 cache support).

Description: Support for these CPUs has been added.

Status: Added (to revision 02.02).

F23 Support for CoreFPGA™, CoreBonito64™, Core20K™.

Description: Support for these core boards has been added.

Status: Added (to revision 02.02).

F24 MIPS16e™, MIPS64™, MIPS3D™, FPU support in disassembly command ("dis").

Description: "dis" command now supports opcodes for these instruction sets/ASEs.

Status: Added (to revision 02.02).

F25 MIPS16e™, FPU support in "gdb" command.

Description: GDB stub now supports the FPU registers.

Copyright © 1999-2011 MIPS Technologies Inc. All rights reserved.

Status: Added (to revision 02.02).

F26 Added "disk" command (IDE Harddisk/Compact Flash support).

Description: Support for IDE harddisks/Compact flash modules on Malta has been added (driver + "disk" command).

Status: Added (to revision 02.02).

F27 Added "cp1" command.

Description: "cp1" command has been added for read/write of FPU control registers.

Status: Added (to revision 02.02).

F28 Support for applications using FPU.

Description: Applications using FPU operations/registers now supported.

Status: Added (to revision 02.02).

F29 Exception dump shows FPU registers.

Description: Exception dump now shows FPU registers if available.

Status: Added (to revision 02.02).

F30 Cache command modified.

Description: Available cache settings are now CPU-specific.

Status: Added (to revision 02.02).

F31 Added '.' command for "dis", "dump" and "eeprom" commands.

Description: More commands may now be "continued" using '.' command. Commands supporting continuation are now "dis", "dump" and "eeprom".

Status: Added (to revision 02.02).

F32 Added "dis" target for makefile (make dis).

Description: "make dis" now generates disassembly files.

Status: Added (to revision 02.02).

Copyright © 1999-2011 MIPS Technologies Inc. All rights reserved.

F33 Code somewhat rearranged in order to make YAMON easier to port.

Description: Various parts of YAMON have been rearranged in order to make it easier to port. In particular, various code has been moved to the ’arch’ directory.

Status: Added (to revision 02.02).

F34 Support for SOC-it 101™ system controller on SEAD-2.

Description: Support for MIPS SOC-it 101 system controller has been added.

Status: Added (to revision 02.03).

F35 Added FPU emulator.

Description: An FPU emulator is added - easy to cut out and port separately.

Status: Added (to revision 02.03).

F36 Added "fread"/"fwrite" commands.

Description: The fread and fwrite commands transfer binary files from/to a tftp server. The commands are later intended to be expanded to IDE disk file transfer.

Status: Added (to revision 02.03).

F37 Added "info sysctrl" command.

Description: Performance related information previously retrieved by the "info memory" command has been moved to this command together with useful information about the system controller (North Bridge).

Status: Added (to revision 02.03).

F38 YAMON is restarted after register dump.

Description: After a register dump has been displayed, YAMON will, after a one seconds delay, attempt to restart the shell prompt. The current command line will be aborted, which means that command line repetition will stop and possible ";" separated commands after the active command will not be invoked.

This feature gives the operator a chance to inspect memory without having to reset the board, once an error has occurred.

Status: Added (to revision 02.03).

F39 Added “startdelay” environment variable to control invocation of "start" command.

Description: An environment variable “startdelay” now exists (default empty string). "startdelay" is a convenient way to either disable the "start" command or to prolongue the initial wait time in seconds before a "start" command is invoked. In case a non empty "start" environment variable exists, the following will apply:

Copyright © 1999-2011 MIPS Technologies Inc. All rights reserved.

- If "startdelay" is unset or empty, YAMON’s initial wait time is 2 seconds for the user to cancel the "start" command.
- If "startdelay" is set to the value "0" (zero), the "start" command will not be invoked at all.
- Otherwise, "startdelay" indicates YAMON’s initial wait time in seconds for the user to cancel the "start" command.

Status: Added (to revision 02.03).

F40 dis command now supports MIPS32/MIPS64 Release 2 instructions.

Description: ’dis’ command now disassembles MIPS32/MIPS64 Release 2 opcodes.

Status: Added (to revision 02.04).

F41 tlb command now supports 1kB pages for MIPS32/MIPS64 Release 2 CPUs supporting small pages.

Description: ’tlb’ command can now be used to setup 1kB pages for MIPS32/MIPS64 Release 2 CPUs that support this. A new option (-s) has been added in order to toggle between using and not using small pages. The shell address validation also handles small pages.

Status: Added (to revision 02.04).

F42 In general CP0 registers are now accessed using 32 or 64-bit operations depending on actual width of register.

Description: According to the MIPS32/MIPS64 architecture definition, it is not allowed to access 64-bit CP0 registers with 32-bit operations (mfc0/mtc0) or 32-bit CP0 registers with 64-bit operations (dmfc0/dmtc0). YAMON now performs 64-bit operations on 64-bit registers and 32-bit operations on 32-bit registers. The ’cp0’ command still allows the user to perform 32 or 64-bit operations any way he wants.

Status: Added (to revision 02.04).

F43 cp0 command and exception handling updated so that only CP0 registers available for the particular CPU are accessed.

Description: According to the MIPS32/MIPS64 architecture definition, it is not allowed to attempt an access to a CP0 register that is not available on a given CPU. Exception handling now only accesses the registers that are available for the CPU. Exception context dumps as well as the ’cp0’ command only present the symbolic names for the registers that are actually available. Any register may still be accessed using the ’cp0’ command by specifying the numeric register value (and select field).

Status: Added (to revision 02.04).

F44 Added support for MIPS32/MIPS64 Release 2 CPU shadow register sets.

Description: YAMON context shift can now handle the case where user application changes the current shadow set. This includes dumping the set in use when an exception occurs as well as communicating the correct values to GDB.

Status: Added (to revision 02.04).

Copyright © 1999-2011 MIPS Technologies Inc. All rights reserved.

F45 Added support for MIPS M4K, 4KSd, 5KE, 5KEf, 25Kf CPUs.

Description: Added support for new CPUs (MIPS M4K, 4KSd, 5KE, 5KEf, 25Kf).

Status: Added (to revision 02.04).

F46 Added support for CoreFPGA-2 Core card.

Description: Added support for new Core card (CoreFPGA-2).

Status: Added (to revision 02.04).

F47 Added support for CoreFPGA rev2 Core card.

Description: Added support for updated Core card (CoreFPGA rev 2).

Status: Added (to revision 02.05).

F48 Added support for MIPS 24K.

Description: Added support for new CPUs (MIPS 24K)

Status: Added (to revision 02.05).

F49 Added support for external interrupt controller (EIC).

Description: Added support for MIPS32R2 external interrupt controller

Status: Added (to revision 02.07)

F50 Improved parsing of environment variables.

Description: Environment variables must now contain alphanumeric and '_' characters. Allow environment variables to be enclosed in braces '{}' so that they may be distinguished from surrounding text.

Status: Added (to revision 02.07)

F51 Support GCC for version 3.x.

Description: The YAMON build system has been updated to support GCC3.x

Status: Added (to revision 02.07)

F52 Added MT/DSP ASE support.

Description: Support for the MT and DSP ASE added to YAMON. Added support for MIPS 34K CPU.

Status: Added (to revision 02.08)

Copyright © 1999-2011 MIPS Technologies Inc. All rights reserved.

F53 Added MIPS 24KE support.

Description: 24KE support added

Status: Added (to revision 02.10)

F54 Added CoreFPGA-3 support.

Description: Added support for the CoreFPGA-3 board

Status: Added (to revision 02.10)

F55 Added Core24KLV support.

Description: Added support for Core24KLV board

Status: Added (to revision 02.11)

F56 Added MIPS 74K support.

Description: 74K support added

Status: Added (to revision 02.11)

F57 Added MIPS L2 cache support.

Description: Support for MIPS32/64 style L2 cache added

Status: Added (to revision 02.11)

F58 Additional SOCit support.

Description: Support for DOCit

Status: Added (to revision 02.13)

F59 Added 24KE cache support.

Description: Support for 24KE cache

Status: Added (to revision 02.13)

F60 Added GIC support.

Description: Added support for new Interrupt Controller (GIC).

Status: Added (to revision 02.14)

Copyright © 1999-2011 MIPS Technologies Inc. All rights reserved.

F61 Added software endian support.

Description: New environment variable softendian allows software or hardware control of board endianness

Status: Added (to revision 02.14)

F62 Added CMP suppor.t

Description: Basic support for the 1004K CMP

Status: Added (to revision 02.15)

F63 Added 74KLV board support.

Description: Basic support for the 74KLV board

Status: Added (to revision 02.17)

F64 Added CPC support.

Description: Basic support for 1004K Cluster Power Controller

Status: Added (to revision 02.17)

F65 Added microMIPS support.

Description: Basic support for the MIPS32/64 microMIPS ASE

Status: Added (to revision 02.17)

F66 Added SEAD-3 board support.

Description: Basic support for the SEAD-3 board added to YAMON

Status: Added (to revision 02.17)

F67 Use highest CAS latency during boot.

Description: Use highest CAS latency during boot. This may affect benchmarks.

Status: Added (to revision 02.17

F68 Added display of additional clock rate multipliers.

Description: Display additional clock rate multipliers

Status: Added (to revision 02.17)

Copyright © 1999-2011 MIPS Technologies Inc. All rights reserved.

F69 Added new support routine for gcc4.

Description: Added new support routine for gcc4

Status: Added (to revision 02.17)

F70 Added NEWSC switch interrupt handling for SEAD-3 boards.

Description: NEWSC switch interrupt handling for SEAD-3 boards

Status: Added (to revision 02.17)

F71 Added SOFTENDIAN support for SEAD-3 boards.

Description: SOFTENDIAN support for SEAD-3 boards

Status: Added (to revision 02.17)

F72 Added SOFTEIC support for SEAD-3 boards.

Description: SOFTEIC support for SEAD-3 boards

Status: Added (to revision 02.17)

F73 Added RTC support for SEAD-3 boards.

Description: RTC support for SEAD-3 boards via PIC32

Status: Added (to revision 02.17)

F74 Added GIC support for SEAD-3 boards.

Description: GIC support for SEAD-3 boards

Status: Added (to revision 02.17)

F75 Added L2 cache resizing support .

Description: L2 cache resizing support

Status: Added (to revision 02.17)

F76 Added message for DSP/MDMX unusable exception.

Description: Message for DSP/MDMX unusable exception.

Status: Added (to revision 02.17)

Copyright © 1999-2011 MIPS Technologies Inc. All rights reserved.

F77 Added ASET and ACLR testing to the test command for SEAD-3 boards..

Description:

Status: Added (to revision 02.18)

F78 Added I_SRAM and D_SRAM support to SEAD-3 boards..

Description:

Status: Added (to revision 02.18)

F79 Added secondary boot loader for SEAD-3 boards (for booting applications such as Linux kernel).

Description:

Status: Added (to revision 02.18)

F80 Added code to allow resetting of the PIC32 chip via the reset register on SEAD-3 boards.

Description:

Status: Added (to revision 02.18)

F81 Changed the default TTY port (ttyS0) to be the USB serial port for SEAD-3 boards.

Description:

Status: Added (to revision 02.18)

F82 Added code to allow user to select the TTY port via the NEWSC buttons on SEAD-3 boards.

Description:

Status: Added (to revision 02.18)

F83 Added code to allow user to reset all environment variables to default via the NEWSC buttons on SEAD-3 boards.

Description:

Status: Added (to revision 02.18)

F84 Added hardware monitoring via the ADT7476 chip on SEAD-3 boards.

Description:

Status: Added (to revision 02.18)

Copyright © 1999-2011 MIPS Technologies Inc. All rights reserved.

F85 Added support for 4K cache and 1074K.

Description:

Status: Added (to revision 02.19)

F86 Added two perl scripts to be used in the release process.

Description:

Status: Added (to revision 02.19)

F87 Added 1 Gigabyte and 2 Gigabyte DIMM support.

Description:

Status: Added (to revision 02.20)

F88 Changed PAUSE_COUNT to permit I2C interface to work with 1GHz processors.

Description:

Status: Added (to revision 02.20)

F89 Added DDR/ECC build when RMW function is turned off for CPU write bursts.

Description:

Status: Added (to revision 02.20)

F90 Enhance RTC initialization.

Description:

Status: Added (to revision 02.20)

F91 Modify PIC32 to function with a 250MHz core on SEAD-3 boards.

Description:

Status: Added (to revision 02.20)

Copyright © 1999-2011 MIPS Technologies Inc. All rights reserved.

Appendix 1

Revision History

Change bars (vertical lines) in the margins of this document indicate significant changes in the document since its last release. Change bars are removed for changes that are more than one revision old.

Revision	Date	Description
01.00	00/01/07	Initial Release
01.01	00/01/13	Added YAMON SEAD 01.00 and YAMON NOLAN 01.00
01.02	00/02/08	Added YAMON 01.01
01.03	00/03/22	Updated copyright notice
02.00	00/09/12	Added YAMON 02.00
02.01	00/09/19	Added error E4
02.02	00/09/26	Added error E5
02.03	01/01/31	Document layout modified
02.04	01/03/27	Added error E6
02.05	01/07/27	Added YAMON 02.02
02.06	01/08/21	Added error E8
02.07	02/09/17	Added YAMON 02.03 and errors E9, E10, E11
02.08	02/11/21	Added YAMON 02.04 (F40..F46 and E12)
02.09	02/12/09	Added E13
02.10	03/12/10	Added YAMON 02.05 (F47..F48 and E14)
02.11	04/03/23	Added YAMON 02.06 (E15, E16)
02.12	04/10/14	Added YAMON 02.07 (F49..F51 and E17)
02.13	05/03/31	Added YAMON 02.08 (F52, E18)
02.14	05/06/15	Added YAMON 02.09 (E19)
02.15	05/10/14	Added YAMON 02.10 (F53,F54)
02.16	06/02/16	Added YAMON 02.11 (E20)
02.17	06/07/04	Added YAMON 02.12 (E21..E23, F55..F57)
02.18	07/11/12	Added YAMON 02.13 (E24, E25, E26, F58, F59) Added YAMON 02.14 (F60, F61)
02.19	07/12/30	Added YAMON 02.15 (F62). No public release.
02.20	08/06/23	Added YAMON 02.16 (E27..E29)
02.21	09/11/6	Added YAMON 02.17 (F63..F76) (E30..E38)
02.22	10/2/6	Added YAMON 02.18 (F77..F84) (E39)
02.23	10/8/3	Added YAMON 02.19 (F85, F86) (E40)
02.24	11/2/15	Added YAMON 02.20 (F87, F88, F89, F90, F91)

Copyright © 1999-2011 MIPS Technologies Inc. All rights reserved.